REMARKS/ARGUMENTS

Claims 1-10, 15, and 16 are pending. Claims 1, 2, 9, and 15 have been amended. Claims 11-14 have been canceled. No new matter has been added.

Claims 1 and 15 were objected for informalities. Claims 1 and 15 have been amended. Claims 1-9 and 11-16 were rejected under 35 U.S.C. § 102(e) as being anticipated by Chang et al. Applicants respectfully traverse the rejection.

The claimed embodiments relate to checking optical proximity correction data using pattern centric methods. Claim 1 recites, "dividing a chip region into at least first and second regions; (b) selecting the first region from the divided regions; (c) providing a first layout database of an integrated circuit design corresponding to the first region, wherein the first layout database is obtained before optical proximity correction treatment; (d) providing a second layout database of the integrated circuit design corresponding to the first region, wherein the second database is obtained after optical proximity correction treatment; (e) finding a location of a first structure in the first layout database; (f) simulating a resulting layout output for the first structure using the second layout database; (g) measuring a first critical dimension of the first structure from the resulting layout output for the first structure; (h) comparing the first critical dimension of the first structure to a drawn dimension of the first structure from the first database; (i) flagging the first structure in the second database if the first critical dimension is less than the first drawn dimension of the first database; (j) repeating the steps (a) to (i) to generate a defect report at least on the first and second regions; (k) analyzing the defect report to identify one or more problematic patterns; and (l) identifying unique patterns from the one or more problematic patterns.

Chang et al. discloses a design rule checking method. Chang et al. does not disclose at least "(k) analyzing the defect report to identify one or more problematic patterns; and (l) identifying unique patterns from the one or more problematic patterns," as recited in claim 1. Claim 1 is allowable. Claim 11-14 have been canceled.

Claim 15 recites, " providing a first layout database of an integrated circuit design, wherein the first layout database is obtained before optical proximity correction

treatment; providing a second layout database of the integrated circuit design, wherein the second database is obtained after optical proximity correction treatment; finding a location of a first structure in the first layout database; finding a first structure in the second layout database based on its location in the first layout database; simulating a resulting layout output for the first structure using the second layout database; measuring a first critical dimension of the first structure from the resulting layout output for the first structure; comparing the first critical dimension of the first structure to a drawn dimension of the first structure from the first database; flagging the first structure in the first database if the first critical dimension is less than the first drawn dimension in the first database to generate a defect report; analyzing the defect report to identify one or more problematic patterns; and identifying unique patterns from the one or more problematic patterns." Chang et al. does not disclose these features. Claim 15 is allowable.

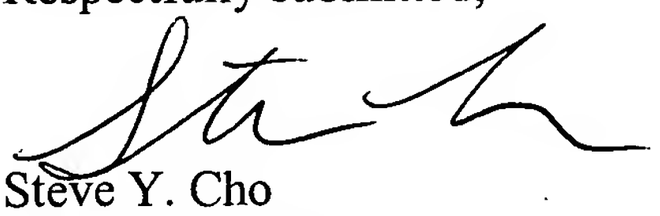
Claims 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chang et al. in view of Garza et al. Applicants respectfully traverse the rejection. Claim 10 depends from claim 1 and is allowable for this reason.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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